CLAIMS

1. An active termination circuit for setting the input impedance of a plurality of input terminals to a predetermined value, the active termination circuit comprising:

a first controllable impedance device coupled between a first supply voltage and a respective one of the input terminals, the impedance of the first controllable impedance device being controlled by a first impedance control signal;

a second controllable impedance device coupled between a second supply voltage and a respective one of the input terminals, the impedance of the second controllable impedance device being controlled by a second impedance control signal;

a first control circuit coupled to provide the first impedance control signal to all of the first controllable impedance devices, the first control circuit comprising:

a third controllable impedance device coupled between a third supply voltage and a first feedback node, the impedance of the third controllable impedance device being controlled by the first impedance control signal;

a first predetermined resistance coupled between the first feedback node and a fourth supply voltage, the third controllable impedance device and the first predetermined resistance forming a voltage divider between the third and fourth supply voltages to produce a first feedback voltage at the first feedback node; and

a first comparator circuit comparing the first feedback voltage to a first reference voltage, the first comparator circuit causing the first impedance control signal to vary so that the first feedback voltage is substantially equal to the first reference voltage; and

a second control circuit coupled to provide the second impedance control signal to all of the second controllable impedance devices, the second control circuit comprising:

a second predetermined resistance coupled between a fifth supply voltage and a second feedback node,

a fourth controllable impedance device coupled between the second feedback node and a sixth supply voltage, the impedance of the fourth controllable impedance device being controlled by the second impedance control signal, the second predetermined resistance and the fourth controllable impedance device forming a voltage divider between the fifth and sixth supply voltages to produce a second feedback voltage at the second feedback node; and

a second comparator circuit comparing the second feedback voltage to a second reference voltage, the second comparator circuit causing the second impedance control signal to vary so that the second feedback voltage is substantially equal to the second reference voltage.

2. The active termination circuit of claim 1, wherein the first, third and fifth supply voltages comprise a power supply voltage, and wherein the second, fourth, and sixth supply voltages comprise ground potential.

3. The active termination circuit of claim 2 wherein the first and second reference voltages comprise one-half the power supply voltage.

4. The active termination circuit of claim 1 wherein the first controllable impedance device and the third controllable impedance device comprise identical controllable impedance devices.

5. The active termination circuit of claim 4 wherein the first controllable impedance device and the third controllable impedance device comprise identical MOSFET transistors.

6. The active termination circuit of claim 1 wherein the second controllable impedance device and the fourth controllable impedance device comprise identical controllable impedance devices.

7. The active termination circuit of claim 6 wherein the first controllable impedance device and the third controllable impedance device comprise identical MOSFET transistors.

8. The active termination circuit of claim 1 wherein:

the first comparator circuit comprises a first differential amplifier generating a first comparison signal corresponding to the difference between the first feedback signal and the first reference signal, the first impedance control signal corresponding to the first comparison signal; and

the second comparator circuit comprises a second differential amplifier generating a first comparison signal corresponding to the difference between the second feedback signal and the second reference signal, the second impedance control signal corresponding to the second comparison signal.

9. The active termination circuit of claim 1 wherein the first controllable impedance device and the third controllable impedance device each comprise a plurality of MOSFET transistors coupled in parallel with each other, and wherein the first impedance control signal selectively turns ON a variable number of the MOSFET transistors in each plurality to alter the impedance of the first and third controllable impedance devices.

10. The active termination circuit of claim 1 wherein the controllable impedance devices comprises respective voltage controlled impedance devices.

11. An active termination circuit for setting the input impedance of a plurality of input terminals to a predetermined value, the active termination circuit comprising:

a first controllable impedance device coupled between a first supply voltage and a respective one of the input terminals, the impedance of the first controllable impedance device being controlled by an impedance control signal;

an impedance device coupled between a second supply voltage and a respective one of the input terminals;

a control circuit coupled to provide the impedance control signal to all of the first controllable impedance devices, the first control circuit comprising:

a second controllable impedance device coupled between a third supply voltage and a feedback node, the impedance of the second controllable impedance device being controlled by the impedance control signal;

a predetermined resistance coupled between the feedback node and a fourth supply voltage, the second controllable impedance device and the predetermined resistance forming a voltage divider between the third and fourth supply voltages to produce a feedback voltage at the feedback node; and

a comparator circuit comparing the feedback voltage to a reference voltage, the comparator circuit causing the impedance control signal to vary so that the feedback voltage is substantially equal to the reference voltage.

12. The active termination circuit of claim 11 wherein each of the impedance devices comprise a third controllable impedance device, the impedance of the third controllable impedance device being controlled by a second impedance control signal.

13. The active termination circuit of claim 11 wherein the first and third supply voltages comprise a power supply voltage, and wherein the second and fourth supply voltages comprise ground potential.

14. The active termination circuit of claim 13 wherein the reference voltage comprise one-half the power supply voltage.

15. The active termination circuit of claim 11 wherein the first controllable impedance device and the second controllable impedance devices comprise identical controllable impedance devices.

16. The active termination circuit of claim 15 wherein the first controllable impedance device and the second controllable impedance device comprise identical MOSFET transistors.

17. The active termination circuit of claim 11 wherein the comparator circuit comprises a differential amplifier generating a comparison signal corresponding to the difference between the feedback signal and the reference signal, the impedance control signal corresponding to the comparison signal.

18. The active termination circuit of claim 11 wherein the first controllable impedance device and the second controllable impedance device each comprise a plurality of MOSFET transistors coupled in parallel with each other, and wherein the impedance control signal selectively turns ON a variable number of the MOSFET transistors in each plurality to alter the impedance of the first and second controllable impedance devices.

19. The active termination circuit of claim 11 wherein the controllable impedance devices comprises respective voltage controlled impedance devices.

20. An active termination circuit for setting the input impedance of a plurality of input terminals to a predetermined value, the active termination circuit comprising:

at least one PMOS transistor coupled between a first supply voltage and a respective one of the input terminals, the impedance of the at least one PMOS transistor being controlled by a first impedance control signal;

at least one NMOS transistor coupled between a second supply voltage and a respective one of the input terminals, the impedance of the at least one NMOS transistor being controlled by a second impedance control signal;

a first control circuit coupled to provide the first impedance control signal to all of the PMOS transistors, the first control circuit comprising:

at least one PMOS transistor coupled between the first supply voltage and a first feedback node, the impedance of the at least one PMOS transistor being controlled by the first impedance control signal;

a first predetermined resistance coupled between the first feedback node and the second supply voltage, the at least one PMOS transistor and the first predetermined resistance forming a voltage divider between the first and second supply voltages to produce a first feedback voltage at the first feedback node; and

a first comparator circuit comparing the first feedback voltage to a first reference voltage, the first comparator circuit causing the first impedance control signal to vary to control the impedance of the at least one PMOS transistor so that the first feedback voltage is substantially equal to the first reference voltage; and

a second control circuit coupled to provide the second impedance control signal to the at least one NMOS transistor, the second control circuit comprising:

a second predetermined resistance coupled between the first supply voltage and a second feedback node,

at least one NMOS transistor coupled between the second feedback node and the second supply voltage, the impedance of the at least one NMOS transistor being controlled by the second impedance control signal, the second predetermined resistance and the at least one NMOS transistor forming a voltage divider between the first and second supply voltages to produce a second feedback voltage at the second feedback node; and

a second comparator circuit comparing the second feedback voltage to a second reference voltage, the second comparator circuit causing the second impedance control signal to vary to control the impedance of the at least one PMOS transistor so that the second feedback voltage is substantially equal to the second reference voltage

21. The active termination circuit of claim 20 wherein the first supply voltages comprises a power supply voltage, and wherein the second supply voltage comprises ground potential.

22. The active termination circuit of claim 21 wherein the first and second reference voltages comprise one-half the power supply voltage.

23. The active termination circuit of claim 20 wherein the at least one PMOS transistor coupled to respective input terminals are substantially to each other and to the at least one PMOS transistor in the first control circuit, and wherein the at least one NMOS transistor coupled to respective input terminals are substantially to each other and to the at least one NMOS transistor in the second control circuit.

24. The active termination circuit of claim 20 wherein the at least one PMOS transistor in the first control circuit and the at least one PMOS transistor coupled to each input terminal each comprise a single PMOS transistor, wherein the at least one NMOS transistor in the second control circuit and the at least one NMOS transistor coupled to each input terminal each comprise a single NMOS transistor, and wherein the first and second impedance control signals comprise respective analog signals.

25. The active termination circuit of claim 20 wherein the at least one PMOS transistor in the first control circuit and the at least one PMOS transistor coupled to each input terminal each comprise a plurality of PMOS transistors coupled in parallel to each other, wherein the at least one NMOS transistor in the second control circuit and the at least one NMOS transistor coupled to each input terminal each comprise a plurality of NMOS transistors coupled in parallel to each other, and wherein the first and second impedance control signals comprise respective signals that selectively turn ON a variable number of the PMOS and NMOS transistors.

26. The active termination circuit of claim 20 wherein:

the first comparator circuit comprises a first differential amplifier generating a first comparison signal corresponding to the difference between the first feedback signal and the first reference signal, the first impedance control signal corresponding to the first comparison signal; and

the second comparator circuit comprises a second differential amplifier generating a first comparison signal corresponding to the difference between the second feedback signal and the second reference signal, the second impedance control signal corresponding to the second comparison signal.

27. A memory device, comprising:

a command decoder receiving memory command signals through externally accessible command input terminals, the command decoder generating memory control signals responsive to predetermined combinations of the command signals;

an address decoder receiving address signals through externally accessible address input terminals, the address decoder generating row and column addressing signals responsive to the address signals;

at least one memory array, the at least one memory array writing data to and reading data from locations corresponding the address signals responsive to the memory control signals;

a data path extending between a plurality of externally accessible data bus terminals and the memory array for coupling data signals to and from the memory array; and

an active termination circuit for setting the input impedance of plurality of the externally accessible terminals to a predetermined value, the active termination circuit comprising:

a first controllable impedance device coupled between a first supply voltage and a respective one of the input terminals, the impedance of the first controllable impedance device being controlled by a first impedance control signal;

a second controllable impedance device coupled between a second supply voltage and a respective one of the input terminals, the impedance of the second controllable impedance device being controlled by a second impedance control signal;

a first control circuit coupled to provide the first impedance control signal to all of the first controllable impedance devices, the first control circuit comprising:

a third controllable impedance device coupled between a third supply voltage and a first feedback node, the impedance of the third controllable impedance device being controlled by the first impedance control signal;

a first predetermined resistance coupled between the first feedback node and a fourth supply voltage, the third controllable impedance device and the first predetermined resistance forming a voltage divider between the third and fourth supply voltages to produce a first feedback voltage at the first feedback node; and

a first comparator circuit comparing the first feedback voltage to a first reference voltage, the first comparator circuit causing the first impedance control signal to vary so that the first feedback voltage is substantially equal to the first reference voltage; and

a second control circuit coupled to provide the second impedance control signal to all of the second controllable impedance devices, the second control circuit comprising:

a second predetermined resistance coupled between a fifth supply voltage and a second feedback node,

a fourth controllable impedance device coupled between the second feedback node and a sixth supply voltage, the impedance of the fourth controllable impedance device being controlled by the second impedance control signal, the second predetermined resistance and the fourth controllable impedance device forming a voltage divider between the fifth and sixth supply voltages to produce a second feedback voltage at the second feedback node; and

a second comparator circuit comparing the second feedback voltage to a second reference voltage, the second comparator circuit causing the second impedance control signal to vary so that the second feedback voltage is substantially equal to the second reference voltage.

28. The memory device of claim 27 wherein the command and address signals are coupled to the memory device in a packet containing both the command signals and the address signals.

29. The memory device of claim 27 wherein the first, third and fifth supply voltages comprise a power supply voltage, and wherein the second, fourth, and sixth supply voltages comprise ground potential.

30. The memory device of claim 29 wherein the first and second reference voltages comprise one-half the power supply voltage.

31. The memory device of claim 27 wherein the first controllable impedance device and the third controllable impedance device comprise identical controllable impedance devices.

32. The memory device of claim 31 wherein the first controllable impedance device and the third controllable impedance device comprise identical MOSFET transistors.

33. The memory device of claim 27 wherein the second controllable impedance device and the fourth controllable impedance device comprise identical controllable impedance devices.

34. The memory device of claim 33 wherein the first controllable impedance device and the third controllable impedance device comprise identical MOSFET transistors.

35. The memory device of claim 27 wherein:

the first comparator circuit comprises a first differential amplifier generating a first comparison signal corresponding to the difference between the first feedback signal and

the first reference signal, the first impedance control signal corresponding to the first comparison signal; and

the second comparator circuit comprises a second differential amplifier generating a first comparison signal corresponding to the difference between the second feedback signal and the second reference signal, the second impedance control signal corresponding to the second comparison signal.

36. The memory device of claim 27 wherein the first controllable impedance device and the third controllable impedance device each comprise a plurality of MOSFET transistors coupled in parallel with each other, and wherein the first impedance control signal selectively turns ON a variable number of the MOSFET transistors in each plurality to alter the impedance of the first and third controllable impedance devices.

37. The memory device of claim 27 wherein the memory device comprises a dynamic random access memory.

38. The memory device of claim 27 wherein the dynamic random access memory comprises a synchronous dynamic random access memory.

39. The memory device of claim 27 wherein the controllable impedance devices comprises respective voltage controlled impedance devices.

40. A memory device, comprising:

a command decoder receiving memory command signals through externally accessible command input terminals, the command decoder generating memory control signals responsive to predetermined combinations of the command signals;

an address decoder receiving address signals through externally accessible address input terminals, the address decoder generating row and column addressing signals responsive to the address signals;

at least one memory array, the at least one memory array writing data to and reading data from locations corresponding the address signals responsive to the memory control signals;

a data path extending between a plurality of externally accessible data bus terminals and the memory array for coupling data signals to and from the memory array; and

an active termination circuit for setting the input impedance of plurality of the externally accessible terminals to a predetermined value, the active termination circuit comprising:

at least one PMOS transistor coupled between a first supply voltage and a respective one of the input terminals, the impedance of the at least one PMOS transistor being controlled by a first impedance control signal;

at least one NMOS transistor coupled between a second supply voltage and a respective one of the input terminals, the impedance of the at least one NMOS transistor being controlled by a second impedance control signal;

a first control circuit coupled to provide the first impedance control signal to all of the PMOS transistors, the first control circuit comprising:

at least one PMOS transistor coupled between the first supply voltage and a first feedback node, the impedance of the at least one PMOS transistor being controlled by the first impedance control signal;

a first predetermined resistance coupled between the first feedback node and the second supply voltage, the at least one PMOS transistor and the first predetermined resistance forming a voltage divider between the first and second supply voltages to produce a first feedback voltage at the first feedback node; and

a first comparator circuit comparing the first feedback voltage to a first reference voltage, the first comparator circuit causing the first impedance control signal to vary to control the impedance of the at least one PMOS transistor so that the first feedback voltage is substantially equal to the first reference voltage; and

a second control circuit coupled to provide the second impedance control signal to the at least one NMOS transistor, the second control circuit comprising:

a second predetermined resistance coupled between the first supply voltage and a second feedback node,

at least one NMOS transistor coupled between the second feedback node and the second supply voltage, the impedance of the at least one NMOS transistor being controlled by the second impedance control signal, the second predetermined resistance and the at least one NMOS transistor forming a voltage divider between the first and second supply voltages to produce a second feedback voltage at the second feedback node; and

a second comparator circuit comparing the second feedback voltage to a second reference voltage, the second comparator circuit causing the second impedance control signal to vary to control the impedance of the at least one PMOS transistor so that the second feedback voltage is substantially equal to the second reference voltage

41. The memory device of claim 40 wherein the command and address signals are coupled to the memory device in a packet containing both the command signals and the address signals.

42. The memory device of claim 40 wherein the first supply voltages comprises a power supply voltage, and wherein the second supply voltage comprises ground potential.

43. The memory device of claim 42 wherein the first and second reference voltages comprise one-half the power supply voltage.

44. The memory device of claim 40 wherein the at least one PMOS transistor coupled to respective input terminals are substantially to each other and to the at

least one PMOS transistor in the first control circuit, and wherein the at least one NMOS transistor coupled to respective input terminals are substantially to each other and to the at least one NMOS transistor in the second control circuit.

45. The memory device of claim 40 wherein the at least one PMOS transistor in the first control circuit and the at least one PMOS transistor coupled to each input terminal each comprise a single PMOS transistor, wherein the at least one NMOS transistor in the second control circuit and the at least one NMOS transistor coupled to each input terminal each comprise a single NMOS transistor, and wherein the first and second impedance control signals comprise respective analog signals.

46. The memory device of claim 40 wherein the at least one PMOS transistor in the first control circuit and the at least one PMOS transistor coupled to each input terminal each comprise a plurality of PMOS transistors coupled in parallel to each other, wherein the at least one NMOS transistor in the second control circuit and the at least one NMOS transistor coupled to each input terminal each comprise a plurality of NMOS transistors coupled in parallel to each other, and wherein the first and second impedance control signals comprise respective signals that selectively turn ON a variable number of the PMOS and NMOS transistors.

47. The memory device of claim 40 wherein:

the first comparator circuit comprises a first differential amplifier generating a first comparison signal corresponding to the difference between the first feedback signal and the first reference signal, the first impedance control signal corresponding to the first comparison signal; and

the second comparator circuit comprises a second differential amplifier generating a first comparison signal corresponding to the difference between the second feedback signal and the second reference signal, the second impedance control signal corresponding to the second comparison signal.

48. The memory device of claim 40 wherein the memory device comprises a dynamic random access memory.

49. The memory device of claim 48 wherein the dynamic random access memory comprises a synchronous dynamic random access memory.

50. A computer system, comprising:

an integrated circuit processor having a plurality of externally accessible terminals coupled to a processor bus;

an input device coupled to the processor through the processor bus adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

an integrated circuit memory device a plurality of externally accessible terminals coupled to a processor bus; and

an active termination circuit coupled to at least some of the externally accessible terminals, the active termination circuit comprising:

a first controllable impedance device coupled between a first supply voltage and a respective one of the externally accessible terminals, the impedance of the first controllable impedance device being controlled by a first impedance control signal;

a second controllable impedance device coupled between a second supply voltage and a respective one of the externally accessible terminals, the impedance of the second controllable impedance device being controlled by a second impedance control signal;

a first control circuit coupled to provide the first impedance control signal to all of the first controllable impedance devices, the first control circuit comprising:

a third controllable impedance device coupled between a third supply voltage and a first feedback node, the impedance of the third

controllable impedance device being controlled by the first impedance control signal;

a first predetermined resistance coupled between the first feedback node and a fourth supply voltage, the third controllable impedance device and the first predetermined resistance forming a voltage divider between the third and fourth supply voltages to produce a first feedback voltage at the first feedback node; and

a first comparator circuit comparing the first feedback voltage to a first reference voltage, the first comparator circuit causing the first impedance control signal to vary so that the first feedback voltage is substantially equal to the first reference voltage; and

a second control circuit coupled to provide the second impedance control signal to all of the second controllable impedance devices, the second control circuit comprising:

a second predetermined resistance coupled between a fifth supply voltage and a second feedback node,

a fourth controllable impedance device coupled between the second feedback node and a sixth supply voltage, the impedance of the fourth controllable impedance device being controlled by the second impedance control signal, the second predetermined resistance and the fourth controllable impedance device forming a voltage divider between the fifth and sixth supply voltages to produce a second feedback voltage at the second feedback node; and

a second comparator circuit comparing the second feedback voltage to a second reference voltage, the second comparator circuit causing the second impedance control signal to vary so that the second feedback voltage is substantially equal to the second reference voltage.

51. The computer system of claim 50 wherein the command and address signals are coupled to the memory device in a packet containing both the command signals and the address signals.

52. The computer system of claim 50 wherein the first, third and fifth supply voltages comprise a power supply voltage, and wherein the second, fourth, and sixth supply voltages comprise ground potential.

53. The computer system of claim 50 wherein the first and second reference voltages comprise one-half the power supply voltage.

54. The computer system of claim 50 wherein the first controllable impedance device and the third controllable impedance device comprise identical controllable impedance devices.

55. The computer system of claim 54 wherein the first controllable impedance device and the third controllable impedance device comprise identical MOSFET transistors.

56. The computer system of claim 50 wherein the second controllable impedance device and the fourth controllable impedance device comprise identical controllable impedance devices.

57. The computer system of claim 56 wherein the first controllable impedance device and the third controllable impedance device comprise identical MOSFET transistors.

58. The computer system of claim 50 wherein:

the first comparator circuit comprises a first differential amplifier generating a first comparison signal corresponding to the difference between the first feedback signal and the first reference signal, the first impedance control signal corresponding to the first comparison signal; and

the second comparator circuit comprises a second differential amplifier generating a first comparison signal corresponding to the difference between the second

feedback signal and the second reference signal, the second impedance control signal corresponding to the second comparison signal.

59. The computer system of claim 50 wherein the first controllable impedance device and the third controllable impedance device each comprise a plurality of MOSFET transistors coupled in parallel with each other, and wherein the first impedance control signal selectively turns ON a variable number of the MOSFET transistors in each plurality to alter the impedance of the first and third controllable impedance devices.

60. The computer system of claim 50 wherein the memory device comprises a dynamic random access memory.

61. The computer system of claim 50 wherein the dynamic random access memory comprises a synchronous dynamic random access memory.

62. The computer system of claim 50 wherein the controllable impedance devices comprises respective voltage controlled impedance devices.

63. A method of controlling the impedance of a plurality of input terminals of an integrated circuit, the method comprising:

comparing the impedance of a first variable impedance device to a predetermined impedance;

coupling each of the input terminals to a respective second variable impedance device; and

based on the comparison, adjusting the impedance of both the first variable impedance device and each of the second variable impedance devices.

64. The method of claim 63, further comprising:

comparing the impedance of a third variable impedance device to a second predetermined impedance;

coupling each of the input terminals to a respective fourth variable impedance device; and

based on the comparison, adjusting the impedance of both the third variable impedance device and each of the fourth variable impedance devices.

65. The method of claim 63 wherein the act of comparing the impedance of a first variable impedance device to a predetermined impedance comprises coupling the first variable impedance device and the predetermined impedance in series with each other between a pair of reference voltages to provide a feedback voltage at a node between the first variable impedance device and the predetermined impedance.

66. The method of claim 65 wherein the act of adjusting the impedance of both the first variable impedance device and each of the second variable impedance devices comprises:

comparing the feedback voltage to a reference voltage;

if the feedback voltage is larger than the reference voltage, adjusting the impedance of both the first variable impedance device and each of the second variable impedance devices in a first direction; and

if the feedback voltage is smaller than the reference voltage, adjusting the impedance of both the first variable impedance device and each of the second variable impedance devices in a second direction that is opposite the first direction.

67. The method of claim 63 wherein the first variable impedance device and the second variable impedance devices each comprise a plurality of fixed impedance devices coupled in parallel with each other, and wherein the act of adjusting the impedance of both the first variable impedance device and each of the second variable impedance devices comprises altering the number of fixed impedance devices coupled in parallel with each other.

68. The method of claim 63 wherein the first variable impedance device and the second variable impedance devices each comprise a plurality of switchable impedance devices coupled in parallel with each other, each of the switchable impedance devices having a low impedance state and a high impedance state, and wherein the act of adjusting the impedance of both the first variable impedance device and each of the second variable impedance devices comprises altering the number of switchable impedance devices having the low impedance state.

69. The method of claim 63 wherein the first variable impedance device and the second variable impedance devices each comprise a continuously variable impedance device, and wherein the act of adjusting the impedance of both the first variable impedance device and the second variable impedance devices comprises continuously varying the impedance of the continuously variable impedance devices.

70. In a memory device, a method of controlling the input impedance of a plurality of externally accessible input terminals, the method comprising:

coupling first and second variable impedance devices to each of the plurality of externally accessible input terminals;

comparing the impedance of one of the first variable impedance devices to a first predetermined impedance;

producing a first feedback signal corresponding to the comparison between the impedance of the first variable impedance device and the first predetermined impedance;

comparing the impedance of one of the second variable impedance devices to a second predetermined impedance;

producing a second feedback signal corresponding to the comparison between the impedance of the second variable impedance device and the second predetermined impedance;

adjusting the impedance of all of the first variable impedance devices as a function of the first feedback signal; and

adjusting the impedance of all of the second variable impedance devices as a function of the second feedback signal.

71. The method of claim 70 wherein the acts of adjusting the impedance of all of the first variable impedance devices as a function of the first feedback signal and adjusting the impedance of all of the second variable impedance devices as a function of the second feedback signal comprise:

comparing the magnitude of the first feedback signal to a first reference voltage;

if the magnitude of the first feedback signal is greater than the first reference voltage, changing the impedance of the first variable impedance devices in a first direction;

if the magnitude of the first feedback signal is less than the first reference voltage, changing the impedance of the first variable impedance devices in a second direction that is different from the first direction;

comparing the magnitude of the second feedback signal to a second reference voltage;

if the magnitude of the second feedback signal is greater than the second reference voltage, changing the impedance of the second variable impedance devices in a first direction; and

if the magnitude of the second feedback signal is less than the second reference voltage, changing the impedance of the second variable impedance devices in a second direction that is different from the first direction.

72. The method of claim 70 wherein the variable impedance devices each comprise a plurality of fixed impedance devices coupled in parallel with each other, and wherein the acts of adjusting the impedance of the variable impedance devices comprise altering the number of fixed impedance devices coupled in parallel with each other.

73. The method of claim 70 wherein the variable impedance devices each comprise a plurality of switchable impedance devices coupled in parallel with each other,

each of the switchable impedance devices having a low impedance state and a high impedance state, and wherein the acts of adjusting the impedance of the variable impedance devices comprise altering the number of switchable impedance devices having the low impedance state.

74. The method of claim 70 wherein the variable impedance devices each comprise a continuously variable impedance device, and wherein the acts of adjusting the impedance of the variable impedance devices comprise continuously varying the impedance of the continuously variable impedance devices.